NanoSpice Pro X

PRIMARIUS

Advanced High Performance FastSPICE Simulator

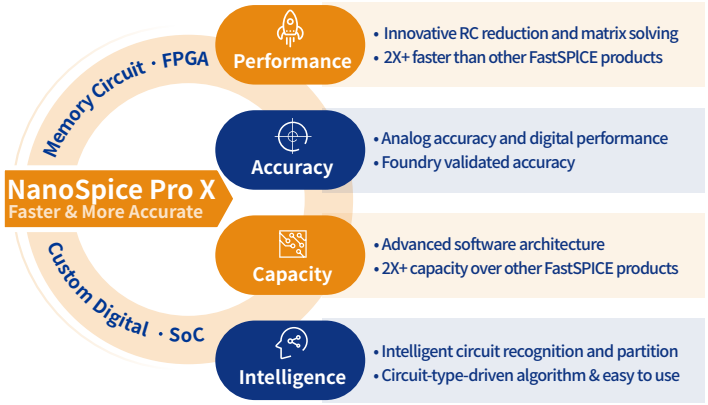
Introduction

To address increasingly stringent accuracy requirements driven by process node advancements and reduced design margins, NanoSpice Pro X employs an adaptive dual-solver technology that seamlessly integrates the state-of-the-art FastSPICE engine and NanoSpice X analog engine to ensure superior analog accuracy and digital performance for memory circuits, CPU, custom digital, SoC and full chip mixed-signal designs.

With its breakthrough FastSPICE algorithm, intelligent topology recognition & automated partition technology, event-driven architecture with enhanced MT scalability, post-layout circuit topology optimization, significantly improved RC reduction capabilities and straight-forward usability based on circuit types, NanoSpice Pro X delivers superiorer performance and capacity than other simulators.

NanoSpice Pro X supports 3D-IC and multi-technology simulation including back-annotation flow. Empowered by the advanced infrastructure, NanoSpice Pro X optimizes outputs and features such as Circuit Check(CCK), ensuring streamlined efficiency while imposing minimal demands on performance and memory consumption.

In synergy with Primarius NanoSpice product family, NanoSpice Pro X provides an one-stop solution for both memory and SoC design.



Key Advantages

- Faster runtime with higher accuracy
  - 2X to 5X over NanoSpice Pro with better accuracy
  - Event driven with better MT scalability
  - Post layout and RC further optimization
- Adaptive dual-solver
  Superior analog accuracy and digital performance
- Breakthrough algorithm
  Circuit detection and auto-partitioning empowered by ML/AI
- Wider coverage
  One stop solution from block level to full chip circuit simulation
- Higher performance
  Advanced infrastructure and efficient output system to minimize cost
- Larger capacity
  2X+ capacity over NanoSpice Pro with over 2 billion elements

Applications

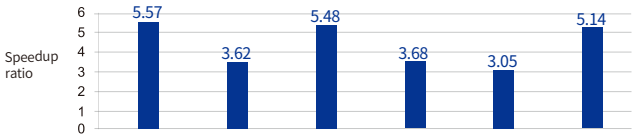
- Flash/DRAM/SRAM function verification, timing & power dissipation
- SRAM characterization
- Complicated mixed signal (ADC, Serdes, PLL) simulation
- Custom digital (CLK Tree, MCU) full chip simulation
- SoC (Transceiver, Display CIS, PMIC, etc.) full chip simulation

Specifications

- Supports Verilog co-simulation
- Supports 3D-IC and multi-technology Simulation (MTS)
- Supports comprehensive Circuit Check (CCK) and Safe Operation Area (SOA)
- Supports SPEF, DSPF, DPF back-annotation
- Unique transient output format - NWF, reduce 2x+ file size
- Supports standard output formats for data analysis:
  FSDB, PSFASCII, SPICEASCII, ASCII, etc
- Supports VEC and VCD stimulus files
- Support public cloud platform,hybrid cloud and private cloud
- Supports S-parameter, Transmission line (W-element, T-element), IBIS model
- Supports HSPICE and Spectre netlist formats
- Supports all public domain models, user-defined models
  - MOSFET: BSIM3, BSIM4, BSIM-BULK, BSIM-IMG, BSIM-CMG, BSIM-SOI, LETI-UTSOI, PSP, HiSIM2, HiSIM_HV, EKV3
  - BJT: MAXTRAM, VBIC, HICUM; TFT: a-Si TFT, poly-Si TFT
  - Diode: JUNCAP, JUNCAP200, DIODE_CMC; Varactor: MOSVAR
  - Resistor: R2_CMC, R3_CMC; HEMT: ASM-HEMT; JFET/MESFET; TMI; Custom PMI; Bsource

Application Examples

NanoSpice Pro X Testcase Data Benchmark



Unit: hours	SRAM Design	SRAM Characterization	DRAM Powerup	DRAM Timing	Flash Full Chip	Flash Module
Ref Simulator	281	263	230	21	189	144
NanoSpice Pro X	50	72	42	5.7	62	28